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Serial Number: **10/699,430**

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 **PALM INTRANET**

Inventor Information for 10/699430

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1	US 7100056 B2	20060829	System and method for managing processor voltage in a multi-processor computer system for optimized performance	713/300	713/320	Barr; Andrew H. et al.
1	US 7080263 B2	20060718	Voltage management of processors in a bladed system based on number of loaded processors	713/300	713/310; 713/320	Barr; Andrew H. et al.
1	US 7076671 B2	20060711	Managing an operating frequency of processors in a multi-processor computer system	713/300	713/322; 713/600	Espinoza- Ibarra; Ricardo et al.
1	US 7058828 B2	20060606	System, method and apparatus for the frequency management of blades in a bladed architecture based on performance requirements	713/320	713/300; 713/322	Barr; Andrew H. et al.
1	US 7055044 B2	20060530	System and method for voltage management of a processor to optimize performance and power dissipation	713/300	713/310; 713/320	Barr; Andrew H. et al.
1	US	20060530	Fan rotor	361/695	361/694;	Espinoza-

	7054156 B2		systems having collapsible fan blades		415/66; 416/1	Ibarra; Ricardo et al.
1	US 7039734 B2	20060502	System and method of mastering a serial bus	710/110	710/119; 710/18	Sun; Weiyun et al.
1	US 6983386 B2	20060103	Voltage management of blades in a bladed architecture system based on thermal and power budget allocation	713/320	307/31; 713/322	Barr; Andrew H. et al.
1	US 6970054 B2	20051129	Apparatus for terminating transmission lines to reduce electromagnetic interference in an electronic system	333/12	333/22R	Cherniski; Andrew Michael et al.
1	US 6961242 B2	20051101	System fan management based on system loading options for a system having replaceable electronics modules	361/695	165/80.3; 361/690; 361/694	Espinoza-Ibarra; Ricardo et al.
1	US 6956344 B2	20051018	High availability fan system	318/538	236/DIG.9; 318/34; 318/445; 416/159; 416/160; 416/162; 417/16	Robertson; Naysen J. et al.
1	US 6948043 B2	20050920	Management of a memory subsystem	711/170	708/309; 708/311; 711/172	Barr; Andrew H. et al.